

**PATENT APPLICATION
1280.SC11318TH**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILING OF A UNITED STATES PATENT APPLICATION

METHOD AND SYSTEM FOR ACCESSING MEMORY DEVICES

INVENTORS:

**Brett W. Murdock
5009 Barlow Drive
Round Rock, TX 78681**

**Craig D. Shaw
12300 Edwards Hollow
Austin, TX 78739**

**Jeremy A. Jacobson
832 Bennington Drive
Crystal Lake, IL 60014**

**ATTORNEY OF RECORD
J. GUSTAV LARSON**

**SIMON, GALASSO & FRANTZ, PLC
P.O. Box 26503
Austin, TX 78755-0503
PHONE (512) 336-8957
FAX (512) 336-9155**

Express Mail Label No. **EL855713396US**

Date of Deposit: 12-27-01

I hereby certify that this paper is being deposited with the U.S. Postal Service
"Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on
the 'Date of Deposit', indicated above, and is addressed to the Commissioner of
Patents and Trademarks, Washington, D.C. 20231.

Name of Depositor: **Terri Alloway**

(print or type)

Signature: *Terri Alloway*

METHOD AND SYSTEM FOR ACCESSING MEMORY DEVICES

FIELD OF THE DISCLOSURE

The disclosures herein relate generally to data processors and more particularly to methods and systems for accessing memory.

BACKGROUND OF THE DISCLOSURE

In many applications, it is expected for a microprocessor to be relatively compact in size, to facilitate expected data processing performance and to support debug functionality. A microprocessor that is relatively compact in size is desirable in embedded system applications such as mobile communication devices and automotive systems. Enabling enhanced utility of on-chip and/or off-chip memory systems and peripheral resources contributes to facilitating exceptional data processing performance. An on-chip debug module provides for effective and efficient debug functionality.

Many integrated processor-based systems, such as micro-controllers, can access word, half-word and byte wide peripherals off-chip. Furthermore, such processor-based systems often include on-chip debug capability. To facilitate data access and debug functionality via such processor-based systems, a conventional processor used in such processor-based systems requires address lines $A[0]$ to $A[n]$, and lane strobes for accessing individual bytes of a word, for example four lane strobes for a 32-bit word, and access size bits (i.e. $SIZ[1:0]$) to indicate a size of an internal access being performed when in debug mode.

However, such flexibility results in unneeded pins for various types of peripheral accesses that do not need to access each byte individually. For example, when accessing a 32-bit word peripheral, the last two address bits (i.e. $A[1:0]$) are not required to designate the specific word to be accessed, while four byte lane strobes are used to access individual bytes of the designated word. When accessing a half-word width peripheral, the last address bit (i.e. $A[0]$) is not required to designate the half word, and only two of the four byte lane strobes are required to

access individual bytes of the designated half word. When accessing a byte width peripheral, the two least significant address bits are used along with one of the four byte lane strobes is required.

Therefore, a system and/or method that reduces the number of device pins while maintaining functionality would be useful.

5

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram view depicting a processor-based system in accordance with an embodiment of the disclosures made herein;

FIG. 2 is a table view depicting a plurality of function modes of the processor-based system depicted in FIG. 1;

FIG. 3 is a block diagram view depicting an external interface module in accordance with an embodiment of the disclosures made herein, wherein the external interface module is connected to a word-wide, half word-wide and byte wide accessible memory module;

FIG. 4 is a block diagram view depicting an external interface module in accordance with an embodiment of the disclosures made herein, wherein the external interface module is connected to a word wide accessible memory module;

FIG. 5 is a block diagram view depicting an external interface module in accordance with an embodiment of the disclosures made herein, wherein the external interface module is connected to a half-word wide accessible memory module;

FIG. 6 is a block diagram view depicting an external interface module in accordance with an embodiment of the disclosures made herein, wherein the external interface module is connected to a byte wide accessible memory module;

FIG. 7 is a block diagram view depicting an external interface module in accordance with embodiments of the disclosures made herein;

FIG. 8 is a block diagram view depicting a multiplex output controller of the external interface module depicted in FIG. 6;

FIG. 9 is a block diagram view depicting a data size register of the external interface module depicted in FIG. 6; and

5 FIG. 10 is a block diagram view depicting an external interface module in accordance with an embodiment of the disclosures made herein, wherein the external interface module is connected to a word-wide, half word-wide and byte wide accessible memories.

DETAILED DESCRIPTION OF THE FIGURES

10 The disclosures made herein relate to data processor-based systems, methods and apparatuses capable of accessing information from external memory and/or peripheral devices. Processor-based systems, methods and apparatuses in accordance with embodiments of the disclosures made herein are useful and advantageous with respect to conventional processor-based systems. Such processor-based systems, methods and apparatuses utilize outputs associated with address bits and byte lane enables to access memory from external devices in a manner that reduces the number of data-processor outputs needed without sacrificing capabilities of the data processor.

15 For purposes of this application, the term lane enable is used generically to describe a signal that is used to indicate a portion of a data word or partial data that is to be accessed. The lane enable can function as a strobe, or clocking-type signal, to provide a timing event to indicate when a portion of the data can be accessed. For example, a lane enable can function as a byte lane strobe during a write to memory, whereby a timing event, such as a rising edge, indicates when a portion of the data word can be written to memory. In another application, the lane enable does not provide any timing events, but instead is used to enable specific data portions to be accessed to and from a memory component or system.

Such data processor-based systems utilize at least a portion of the data processor's outputs in a plurality of different manners depending on a particular mode of operation of the processor. For example, in accordance with at least one embodiment of the disclosures made herein, a first output provides a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address when in a first mode of operation, and the first output provides an address bit of a second memory address for facilitating designation of a second memory storage location when in a second mode of operation. In this manner, relative to conventional data processors and data processor-based systems, fewer processor output pins are required for providing a prescribed set of functionality.

FIG. 1 depicts a processor-based system 100 in accordance with an embodiment of the invention. The processor-based system 100 includes a data processor 101, and an external memory module 124. Data processor 101 further includes a processing module 102, an on-chip memory module 104, an integrated interface module 106 and a plurality of peripheral modules 108. A first communication bus 110 is connected between the processing module 102, the on-chip memory module 104 and the integrated interface module 106. A second communication bus 112 is connected between the integrated interface module 106 and each one of the plurality of peripheral modules 108. It will be appreciated that in specific embodiments of the disclosure made herein that the various components may be coupled to each other through other intermediary components not illustrated. For example, the integrated interface module 218 may be coupled to the external memory module 124 through output drivers not illustrated.

The processing module 102 includes an integrated debug module 114. The integrated debug module 114 supports debug and/or emulation functionality such as de-bug registers that enable a developer to identify data corruption problems by monitoring data read and write accesses to program variables and instructions. Data processors including integrated debug modules are commercially available from a variety of sources. For example, an M-CORE processor offered by Motorola is an example of a data processor including an integrated debug module.

The integrated interface module 106 includes peripheral interface controller 116 and an external interface module 218. The peripheral interface controller 116 comprises a peripheral interface 120 and an interrupt controller 122. The external interface module 218 is connected to an external memory module 124 via a third communication bus 126 for providing interface functionality between the data processor 101 and the external memory module 124. The external memory module is an example of an external peripheral, which may be a primary data storage device, such as a Dynamic Random Access Memory (DRAM) or a Static Random Access Memory, or an external device that can gather or otherwise determine data values that are to be accessed by the data processor 100.

The peripheral interface 120 facilitates interface functionality between the plurality of peripheral modules 108 and the integrated interface module 106. Each one of the peripheral modules 108 includes a respective module interface 128 for supporting such interface functionality between the plurality of peripheral modules 108 and the integrated interface module 106. The interrupt controller 122 facilitates interrupt functionality between the plurality of peripheral modules 108, the processing module 102, and the integrated interface module 106. The peripheral interface controller 116 and the external interface module 218 are connected to each other via the first communication bus 110. Furthermore, the peripheral interface controller 116 and the external interface module 218 are connected to the processing module 102 and the on-chip memory module 104 via the first communication bus 110.

In accordance with embodiments of the invention disclosed herein, the external interface module 218 supports functionality of a plurality of multiplexed outputs (i.e. multiplexed outputs A[z:w]) to access the external memory module 124 in addition to conventional chip select and memory address functionality. By multiplexed outputs, it is meant that an output of data processor 101 has a plurality of different functionalities associated therewith. Examples of such different functionalities include providing byte lane enable functionality and providing address bit functionality.

FIG. 2 depicts a plurality of functional modes associated with multiplexed outputs A[z:w] in accordance with embodiments of the disclosures made herein. In one embodiment, a specific

mode of operation can be indicated by a value stored in a data size register of the data processor 101. For example, data size values, as indicated in the DSZ column of the table of FIG. 2 can be used indicate a specific mode of operation.

As depicted in FIG. 2, the functionality of the multiplexed outputs A[z:w] is dynamic by access in that the functionality of the multiplexed outputs A[z:w] can vary for each external device being accessed. For example, the data processor 101 can interface with a first external memory device to operate in a first functional mode, where the multiplexed output A[x] provides byte lane enable functionality (i.e. EB[1]) for facilitating access of a portion of a first memory storage location of the first external memory device, where the first storage location is designated by address data. A second external memory device can be controlled by the data processor 101 to operate in a second functional mode, where the multiplexed output A[x] provides least significant address bit functionality (i.e. A[0] and A[1]) for facilitating designation of a memory storage location within the second external memory device. A third external memory device can operate in a third functional mode, where multiplexed output A[x] provides most significant address bit functionality (i.e. A[n+1]) for facilitating designation of a memory storage location within the third external memory device, thus expanding the addressable memory depth from n addresses to n+1 addresses.

As illustrated in the table of FIG. 2, four different 8-bit modes of operation allow multiplexed outputs A[w], A[x], A[y] and A[z] to provide byte lane enable functionality EB[0], EB[1], EB[2] and EB[3], respectively, wherein each one of the multiplexed outputs A[z:w] enables access of a different byte of data (i.e. D[7:0], D[15:8], D[23:16], D[31:24]) where multiple byte wide memory devices are used (see FIG. 5). In a half-word wide memory access, such as the 16 bit modes of operations of FIG. 2, a first two of the multiplexed outputs A[z:w] enable access of a first half word of data (i.e. D[31:16]) and a second two of the multiplexed outputs A[z:w] enable access of a second half word of data (i.e. D[15:0]), as shown in FIG. 4. In a word wide memory access, such as the 16-bit modes of operations of FIG. 2, all four of the multiplexed outputs A[z:w] enable access of a word of data (i.e. D[31:0]). In at least one embodiment of a word wide memory, the number of bits associated with such a word wide memory is greater than 8. Note that the data enables EB[3:0] can be read and/or write enables

used to access a specific portion of data, such as a byte, associated with a specific access. In one embodiment, the enables EB[3:0] are specifically write enables, while the access of a portion of data word is handled within the data processor 101 after an entire word is received.

When the processor-based system 100 is in a debug mode, the byte lane enable functionality provided by the multiplexed outputs A[z:w] facilitates determining a size and least significant address bits of an internal access being performed. In at least one embodiment of the disclosures made herein, the debug mode (i.e. a show-cycles mode) is recognized when the address bits and multiplexed outputs A[z:w] are active, but no chip selects are present to indicate an external access.

FIG. 3 illustrates a system where a data processor 101 is coupled to external memories 140, 142 and 144. In the embodiment illustrated, memory 140 is a memory module that provides data access using one or more word wide memory devices that are selected by chip select CS[0], memory 142 is a memory module that provides data access using one or more pairs of half-word wide memory devices that are selected by chip selects CS[1] and CS[2], memory 144 is a memory module that provides data access using one or more sets of four byte wide memory devices that are selected by chip selects CS[3], CS[4], CS[5] and CS[6]. Memory modules 140, 142 and 144 are further illustrated in FIGS. 5, 6 and 7, respectively.

FIG. 4 illustrates the connections between memory 140 and the data processor 101 in greater detail. Note that where appropriate the nodes within memory 140 are labeled with the generic names (A[w:z]) and the functional names (EB[3:0], CS[0]). In operation, CS[0] is asserted to enable access of the memory device 230. Accordingly, the functionality of the multiplexed outputs A[w:z] is according to the specific mode of operation associated with CS[0]. For example, a DSZ register associated with CS[0] can be used to specify an appropriate 32-bit mode of operation. In the embodiment illustrated, the multiplexed outputs A[w:z] to device 230 act as lane enables EB[3:0], respectively, as illustrated in the table of FIG. 2.

FIG. 5 illustrates the connections between memory 142 and the data processor 101 in greater detail. Note that where appropriate the nodes within memory 142 are labeled with their generic names (A[w:z]) and their functional names (EB[3:0], A[1], A[n+1]). In operation CS[1]

is asserted to enable access of memory device 232, and CS[2] is asserted to enable access of memory device 234. Accordingly, the functionality of the multiplexed outputs A[w:z] is determined according to specific mode of operation associated with CS[1] and CS[2] respectively. For example, a DSZ register associated with CS[1] can be used to specify an appropriate 16-bit mode of operation, while a different DSZ register associated with CS[2] can be used to specify the same or a different 16-bit mode of operation. In the embodiment illustrated, the multiplexed outputs A[w:z] to device 232 act as EB[1:0], A[1], and A[n+1], respectively, as illustrated in the table of FIG. 2.

FIG. 6 illustrates the connections between memory 144 and the data processor 101 in greater detail. Note that where appropriate the nodes within memory 144 are labeled with their generic names (A[w:z]) and their functional names (EB[4:0], A[0], A[1], A[n+1]). In operation CS[3] is asserted to enable access of memory device 236, CS[4] is asserted to enable access of memory device 238, CS[5] is asserted to enable access of memory device 240, CS[6] is asserted to enable access of memory device 242. Accordingly, the functionality of the multiplexed outputs A[w:z] is determined according to specific mode of operation associated with CS[3], CS[4], CS[5] and CS[6] respectively. For example, a DSZ register associated with CS[3] can be used to specify an appropriate 16-bit mode of operation, while a different DSZ register associated with CS[4] can be used to specify the same or a different 16-bit mode of operation. In the embodiment illustrated, the multiplexed outputs A[w:z] to device 236 act as EB[3], A[1:0], and A[n+1], respectively, as illustrated in the table of FIG. 2.

The data processor 101 is a component of a processor-based system, such as system 100, in accordance with an embodiment of the disclosures made herein. The processor-based system 101 depicted in FIG. 1 is an example of such a processor-based system. The data processor 101 facilitates address generation functionality (e.g. A[n:2], A[n+1:2]), chip select functionality (i.e. CS[5:0]), byte lane enable functionality (i.e. A[z:w]) and data transmission functionality (i.e. Data[31:0]).

In accordance with embodiments of the disclosures made herein, at least one of the multiplexed outputs A[z:w] is capable of providing byte lane enable functionality and address bit

functionality depending on a mode of operation. Furthermore, the processor-based system comprising the external interface module 218 may be connected to a debug monitor system which will debug the multiplexed outputs A[z:w] when an internal access is being displayed on the external address and data busses. For example, if no chip select is externally active, and the address and data bus, and any corresponding control signals, are being asserted, an external debug monitor system will assume that an internal access is occurring and use the external signals to monitor the internal data accesses. In one embodiment, the multiplexed outputs indicate what bytes of data are being accessed by an internal access. From this data, the debug monitor can determine a size and location for a specific address A[n:2].

FIG. 7 depicts various functional components of the external interface module 218 of FIG. 1 that can be used to implement the functionality described with reference to the table of FIG. 2. The external interface module 218 includes a multiplex output controller 250, an address generator 252, a lane enable generator 254 and a data size register module 256. The address generator 252, the lane enable generator 254 and the data size register module 256 are each connected to the multiplex output controller 250.

In response to receiving a module address from one of the peripheral modules of FIG. 1, the address generator 252 and the lane enable generator 254 generate appropriate address bits A[0:n+1] and byte lane enables S[0:3], respectively. Bits that are subject to being multiplexed A[0], A[1], A[n:2], A[n+1], S[0], S[1], S[2] and S[3]) are provided to the multiplex output controller. In response to the data size register module 256 receiving a register select, the data size register module 256 will determine corresponding DSZ bits which are used to provide the data signals A[0], A[1], A[n+1], S[0], S[1], S[2] and S[3] to the appropriate output location. As discussed above in reference to FIG. 2, the address bit A[n+1] expands the addressable memory depth of a processor based system when a specific access does not require four pins for least significant address bits or a lane enable.

As depicted in FIG. 8, in accordance with at least one embodiment of the disclosures herein, the multiplex output controller 250 includes a first multiplexer 260, a second multiplexer 262, a third multiplexer 264, a fourth multiplexer 266 and a DSZ decode module 268. Each one

of the multiplexers (260-266) has an output corresponding to a respective one of the multiplexed outputs A[z:w] and has a plurality of inputs connected thereto. The DSZ decode module 268 is capable of providing a control signal (i.e. one or more a control bits) to each one of the multiplexers (260-266). In response to the DSZ decode module receiving a DSZ input (i.e. DSZ bits) from the data size registers 256, the DSZ decode module 268 uses the DSZ signal for determining which one or more of the multiplexers (260-266) receives a corresponding control signal and subsequently provides such one or more of the multiplexers (260-266) with the corresponding control signal. The function of the data size registers 256 is discussed below in reference to FIG. 8.

The first multiplexer 260 is a two input multiplexer providing an output associated with a first one of the multiplexed outputs A[z:w] (i.e. the first multiplexed output A[w]). The output provided by the first multiplexer 260 is provided at an output node 261. A first address bit A[0] and a first byte lane enable EB[0] are provided as inputs to the first multiplexor 260. A first control signal A[wc] is provided by the DSZ decode module 268 to the first multiplexer 260 for determining which input is provided as the output from the first multiplexer 260.

The second multiplexer 262 is a four input multiplexer providing an output associated with a second one of the multiplexed outputs A[z:w] (i.e. the second multiplexed output A[x]). The output provided by the second multiplexer 262 is provided at a third output node 263. The first address bit A[0], a second address bit A[1], a second byte lane enable EB[1] and a third address bit A[n+1] are provided as inputs to the second multiplexor 262. A second control signal A[xc] is provided by the DSZ decode module 268 to the second multiplexer 262 for determining which input is provided as the output from the second multiplexer 262.

The third multiplexer 264 is a three input multiplexer providing an output associated with a third one of the multiplexed outputs A[z:w] (i.e. the third multiplexed output A[y]). The output provided by the third multiplexer 264 is provides at a third output node 265. The second address bit A[0], a third byte lane enable EB[2] and the third address bit A[n+1] are provided as inputs to the third multiplexor 264. A third control signal A[yc] is provided by the DSZ decode module

268 to the third multiplexer 264 for determining which input is provided as the output from the third multiplexer 264.

The fourth multiplexer 266 is a two input multiplexer providing an output associated with a fourth one of the multiplexed outputs A[z:w] (i.e. the fourth multiplexed output A[z]). The output provided by the fourth multiplexer 264 is provided at a fourth output node 267. A fourth byte lane enable EB[3] and the third address bit A[n+1] are provided as inputs to the fourth multiplexer 266. A fourth control signal A[zc] is provided by the DSZ decode module 268 to the fourth multiplexer 266 for determining which input is provided as the output from the fourth multiplexer 266.

As depicted in Fig. 8, in accordance with at least one embodiment of the disclosures herein, the data size register module 256 includes a plurality of data size (DSZ) registers 280 and a DSZ selector 282 connected to each one of the data size registers 280. In response to receiving a given register select signal, the DSZ selector 282 facilitates determining a corresponding data size register and providing data size bits (i.e. DSZ bits [2:0]) associated with the corresponding data size register to the DSZ decode module 268 of the multiplex output controller 250. In one embodiment, a chip select signal being asserted, or to be asserted, can be used as the register select. Specific embodiments of the DSZ bits [2:0] and the resulting functionality of the multiplexed outputs A[z:w] are depicted in FIG. 2. Determining data size bits associated with a specific register select is an example of determining a mode of operation for at least one of the multiplexed outputs A[z:w].

FIG. 9 illustrates the Data size register module 256 of FIG. 7 in greater detail. Specifically, the Data size register module 256 of FIG. 9 illustrates a plurality of data size registers 280 connected to a DSZ selector 282. The data stored within one of the data size registers is provided at the output of the DSZ selector 282, as data DSZ[2:0], based upon a register select signal. One embodiment, the register select signal is based upon a chip select signal. For example, if CS4 is to be asserted, the value stored in DSZ[4] will be provided at the output of the selector 282. In this manner, the functionality of the multiplexed outputs A[z:w] can be dynamic based on the active chip select.

It will be appreciated because the functionality of the multiplexed output $A[w:z]$ varies on an access by access basis, depending upon a specific chip select, that additional timing consideration may need to be considered. For example, if a specific multiplexed output is changing its functionality from being an address output to being a lane enable output, it will generally be necessary to avoid any race condition that would allow the address data of the previous state from being interpreted as an active enable signal of a subsequent state. This can be accomplished by making sure that when a new chip select is to be asserted, indicating a functional transition in the multiplexed outputs that it does so after the multiplexed output data has transitioned. For example, a half-cycle, or more, of delay can be added between when the multiplexed outputs change and when a new chip select is asserted. It will be appreciated, that the system can also be designed to assure no race condition will exist without the addition extra clock cycles.

FIG. 10 illustrates system 300 having a data processing device 301, similar to device 101, coupled to one word wide device 240, one half-word wide device 242, and one byte wide device 244. Chip selects CS0, CS1, and CS2 enable the devices 240, 242, and 244 respectively. Multiplexed output $A[w]$ is connected to devices 240, 242, and 244 to operate as a lane enable, another lane enable, and the address bit $A[0]$, respectively. Multiplexed output $A[x]$ is connected to devices 240, 242, and 244 to operate as a lane enable, another lane enable, and the address bit $A[1]$, respectively. Multiplexed output $A[y]$ is connected to devices 240, 242, and 244 to operate as a lane enable, another lane enable, $A[1]$, and $A[n+1]$, respectively. Multiplexed output $A[z]$ is connected to devices 240, 242, and 244 to operate as a lane enable, $A[n+1]$, and a lane enable, respectively. As indicated, the system 300 is designed to have memory 242 access data on $DATA[15:0]$, while memory 242 will access data on $DATA[7:0]$.

It should be understood that the specific steps indicated herein, and/or the functions of specific modules herein, may be implemented in hardware and/or software. For example, a specific step or function may be performed using software and/or firmware executed on one or more a processing modules. In addition, the logic functions performed by hardware representations herein, such as the multiplexers of FIG. 8 can be implemented in a variety of manners. For example, it will be appreciated that the illustrated multiplexer of FIG. 8 can be

implemented using various hardware or software implementations that route data in the manner described.

For example, a system for accessing memory devices as described herein may include a generic processing module and memory. The processing module can be a single processing device or a plurality of processing devices used to determine the data bits to be provided to the multiplexed outputs A[w:z]. Such a processing device may be a microprocessor, microcontroller, digital processor, microcomputer, a portion of a central processing unit, a state machine, logic circuitry, and/or any device that manipulates the signal.

The manipulation of signals by a processing device, such as a microprocessor, is generally based upon operational instructions represented in a memory. The memory may be a single memory device or a plurality of memory devices. Such a memory device may be a read only memory, a random access memory, a floppy disk memory, magnetic tape memory, erasable memory, a portion of a system memory, and/or any device that stores operational instructions in a digital format. Note that when the processing module implements one or more of its functions, it may do so where the memory storing in the corresponding operational instructions is embedded within the circuitry comprising a state machine and/or other logic circuitry.

In the preceding detailed description, reference has been made to the accompanying drawings that form a part hereof, and in which are shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments and certain variants thereof, have been described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other suitable embodiments may be utilized and that logical, mechanical, chemical and electrical changes may be made without departing from the spirit or scope of the invention. For example, the invention has been described with respect to a 32-bit word and byte wide enables, however, it will be appreciated that other word and lane strobe widths can be used, and that a word of memory as claimed includes not only a word width of 32 bits, but other word widths as well. In addition, it will be appreciated that the functional blocks shown in the figures could be further combined or divided in a number of manners without departing from the spirit or scope of the invention. The preceding detailed description

is, therefore, not intended to be limited to the specific forms set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the appended claims.

11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
2224
2225
2226
2227
2228